Module 13: **CMOS cell layout 1**

Learning objectives:

Study of the following topics –

CMOS layout rules

CMOS inverter layout

Layout of CMOS NAND, NOR and AND gates

This module is the first of two dealing with the layout of digital circuits in CMOS technology. The importance of IC layout is discussed first as the logical succession from CMOS circuit design and simulation. CMOS layout ideas and rules are discussed next followed by the example of a CMOS inverter layout. The topic of shared area between adjacent devices is discussed next. Finally, the layout of CMOS NAND, NOR and AND gates are described.

First go through the Powerpoint slides and the videos and then complete the associated reading assignments for this module.

Reading assignments

Download and read the following article:

http://www.eda-utilities.com/CMOS\_Transistor\_Layout\_KungFu.pdf

Questions

Q1. Sketch a CMOS layout for the XOR function.

Q2. Sketch CMOS layout for a two 2-input AND gates with their outputs connected to a 2-input OR gate. Do this using both AND and OR gates and then using only NAND gates.